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EXAMINER
PHAM, THANHHA S

ART UNIT	PAPER NUMBER
2813	5

DATE MAILED: 11/20/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/976,635	TRIVEDI, JIGISH G.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action responses to Applicant's amendment Paper No. 4 dated 8/9/02.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 1-4, 5-12, 13-16, 26 and 32-39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1,

Line 10, "the isolation material" lacking antecedent basis should be change to "the first trench isolation material"

lines 17-18, "the substrate" lacking antecedent basis should be changed to "the semiconductor substrate"

With respect to claim 5,

Line 6, "the isolation material" lacking antecedent basis should be change to "the first trench isolation material"

Lines 11-12, "the substrate" lacking antecedent basis should be changed to "the semiconductor substrate"

With respect to claim 3,

"the forming conductive material within the line trench" lacking antecedent basis should be changed to "the depositing conductive material within the trench"

With respect to claim 4,

Lines 2-3, "the isolation material proximate active area substrate material" renders the claim indefinite. It is not clear how to define the locations of "the isolation material" and "active area substrate material" so that the trench isolation material can be considered to be proximate active area substrate material.

With respect to claim 6,

"the substrate" lacking antecedent basis should be changed to "the semiconductor substrate"

With respect to claim 13,

Lines 5-6, "the isolation material" lacking antecedent basis should be changed to "the trench isolation material"

Line 7, it is not clear that "the trench" refers to which trench – the isolation trench or the line trench?

With respect to claim 16,

Line 2, "the conductive material" renders the claim indefinite. It is clear that "the conductive material" is the first conductive material or the second material.

With respect to claim 26,

"the substrate" lacking antecedent basis should be changed to "the semiconductor substrate.

With respect to claim 32,

Lines 4-5, "an edge of the trench isolation material proximate active area substrate material" renders the claim indefinite. It is not clear how to define the locations of "an edge of the isolation material" and "active area substrate material" so that an edge of the trench isolation material can be considered to be proximate active area substrate material.

With respect to claim 36,

Lines 4-5, "an edge of the trench isolation material proximate active area substrate material" renders the claim indefinite. It is not clear how to define the locations of "an edge of the isolation material" and "active area substrate material" so that an edge of the trench isolation material can be considered to be proximate active area substrate material.

Line 7, "the trench" lacking antecedent basis should be changed to " the line trench"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 23 and 27-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim [US 5,573,969].

Kim, figs 3's and text col 1-3, discloses the claimed method of forming a local interconnect comprising:

providing a bulk semiconductor substrate having a first conductivity type background region (10, fig 3A, col 1 lines 64-67 and col 2 lines 1-11 & 59-60), an adjacent second conductivity type background region (20) and a boundary extending therebetween;

forming an isolation trench (30, fig 3A, col 2 lines 60-61) within the bulk semiconductor substrate over and along the boundary, the isolation trench having opposing longitudinal sidewalls in at least one cross section, the isolation trench being laterally centered over the boundary;

depositing a trench isolation material (31, fig 3A, col 2 lines 60-64) over the bulk semiconductor substrate and to within the isolation trench;

removing the trench isolation material effective to form a line trench (7, fig 3C) within isolation material into a desired local interconnect configuration, the line trench being laterally centered over the boundary and centered between longitudinal sidewalls of the isolation trench in at least one cross section; and

forming conductive material (35, fig 3E, col 3 lines 37-42) to within the line trench.

3. Claims 23, 27-32 and 36, as being best understood, are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ochii [US 4,661,202].

Ochii, fig 7 and text col 1-8, discloses the claimed method for forming a local interconnect comprising:

providing a bulk semiconductor substrate having a first conductivity type background region (22, fig 7), an adjacent second conductivity type background region (23) and a boundary extending therebetween;

forming an isolation trench (50, fig 7, col 5 lines 64-68 and col 6 lines 1-5) within the bulk semiconductor substrate over and along the boundary, the isolation trench having opposing longitudinal sidewalls in at least one cross section, the isolation trench being laterally centered over the boundary;

depositing a trench isolation material (51) over the bulk semiconductor substrate and to within the isolation trench;

etching a line trench (trench for depositing conductive material 52, fig 7, col 4 lines 39-43) into a desired line configuration with the trench isolation material (51) formed relative to a bulk semiconductor substrate, the line trench in the trench isolation material not extending to an edge of the trench isolation material adjacent active area substrate material (22 and 23), the line trench being laterally centered over the boundary and centered between longitudinal sidewalls of the isolation trench in at least one cross section;

depositing conductive material (52, fig 7) to within the line trench;

forming insulating material (37, fig 7) over the trench isolation material (51) and over the conductive material (52);

etching a contact opening (fig 7, col 4 lines 65-68 and col 5 lines 1-5) into the insulating material which bridges over and between said active area substrate material (22 , fig 7); and

forming a conductor (39b, fig 7) within the contact opening which electrically connects said conductive material (52) with said active area substrate material (22).

4. Claims 13-14, 17-20, 23-25, 32 and 34-35, as being best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Yagishita et al [US 6,346,438].

Yagishita et al, figs 3's-6 and related text col 1-29, discloses the claimed method of forming a local interconnect comprising:

forming an isolation trench (14, fig 3B) within a semiconductor substrate (15);

depositing a trench isolation material (16, fig 3C) over the semiconductor substrate and to within the isolation trench;

removing/etching trench isolation material effective to form a line trench (17, fig 3D) within the trench isolation material into a desired local interconnect configuration, the line trench being laterally centered between sidewalls of the isolation trench in at least one cross section;

forming an oxidation resistant liner layer (24, silicon nitride, fig 6, col 7 lines 15-16) and a conductive lining of first conductive material (TiN, col 7 lines 16-18) within the line trench for lining within the line trench; and

depositing a second conductive material (25, W, fig 6) different from the first conductive material on the conductive lining and to within the trench line, and recessing the second conductive material after depositing the second conductive material (col 7 lines 22-35).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 26, 33 and 39, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochii [4,661,202], Kim [US 5,573,969] or Yagishita et al [US 6,346,438] as applied to claims 23, 32 or 36 above, in further view of Wolf et al ["Silicon Processing For the VLSI ERA", Vol 1 Process technology, pp 5-6, Lattic Press 1986].

Ochii, Kim and Yagishita et al substantially discloses the claimed method but is silent about the teaching of using the semiconductor substrate of monocrystalline substrate.

However, Wolf et al shows that utilizing monocrystalline substrate keeps an important role in forming a semiconductor device due to its high crystalline perfection and uniformity of structure. In addition, using such as semiconductor substrate with

moncrystalline structure has been well-known in the art of forming a semiconductor device.

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Wolf et al to the process of Ochii, Kim or Yagishita et al use the semiconductor substrate of monocrystalline substrate for forming a better semiconductor device with reasons given above.

7. Claims 15-16 and 21-22, as being best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Yagishita et al [US 6,346,438] in view of Huang [US 2001/0003663]

Yagishita et al substantially discloses the claimed method including depositing the second conductive material to within the line trench and covering the second conductive material with insulative material wherein at least some of the insulative material being received within the line trench. Yagishita does not expressly teach said insulative material being the same as the trench isolation material.

However, selection of such known material based on its suitability for its intended use is prima facie obvious (see Sinclair & Carroll Co., Inc. v. Interchemical Corp. , 325 U.S. 327, 65 USPQ 297 (1945)). See Huang as an evidence that teaches using the insulative material (20, silicon oxide, fig 1) to protect the second conductive material (18) wherein the insulative material (20) being the same as the trench isolation material (12, silicon oxide).

Therefore, it would have been obvious for those skilled in the art to select the insulative material the same as the trench isolation material as a suitable material in the process Yagishita et al for protecting the second conductive material.

8. Claims 24, 34 and 37are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochii as applied to claims 23, 32 and 36 above, and further in view of Kim et al [US 6,133,116].

Ochii substantially discloses the claimed method except teaching recessing the conductive material after depositing the conductive material in the trench line.

Kim teaching recessing the conductive material (214a, fig 8F) after depositing the conductive material in the line trench (210) for providing spaces to deposit insulating material (216) for protecting the conductive material in the line trench.

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Kim to the process of Ochii to recess the conductive material as being claimed to provide spaces for forming further insulating material to protect the conductive line when a design of the device is needed.

9. Claims 25, 35 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochii as applied to claim23, 32 and 37 above, and further in view of Huang et al [US 6,027,994].

Ochii substantially discloses the claimed method except teaching forming the conductive material within the trench line comprises depositing at least two conductive materials .

However, using the two conductive materials in a trench line for local interconnection is well-known in the art. See Huang et al as an evidence that teaches forming the conductive material using at least two conductive material (barrier/glue conductive layer 135 and conductive metal 140) in the trench line to provide a better interconnection without problem of peeling.

Therefore, it would have been obvious for those skilled in the art to combine the teaching of Huang et al to the process of Ochii to use at least two conductive material as being claimed to provide a better interconnection with reasons given above.

Allowable Subject Matter

10. Claims 1-12 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

11. The following is a statement of reasons for the indication of allowable subject matter: Independent claims 1 and 5 recites the steps for forming local interconnect comprising: depositing a first trench isolation material over the semiconductor substrate and to within the isolation trench; removing first isolation material effective to form a line trench within the isolation first trench isolation material into a desired local interconnect configuration; forming conductive material within the line trench; depositing a second trench isolation material over the first trench isolation material, over the conductive material within the isolation trench and within the line trench; and removing at least some first and second trench isolation material form the semiconductor substrate in at

least one common removing step. However, such a combination of step is not suggested or taught by prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (703) 308-6172. The examiner can normally be reached on Monday-Thursday 8:00 AM - 7:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr., can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-3432 for regular communications and (703) 308-7725 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Thanhha Pham
November 15, 2002

Carl Whitehead Jr.
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